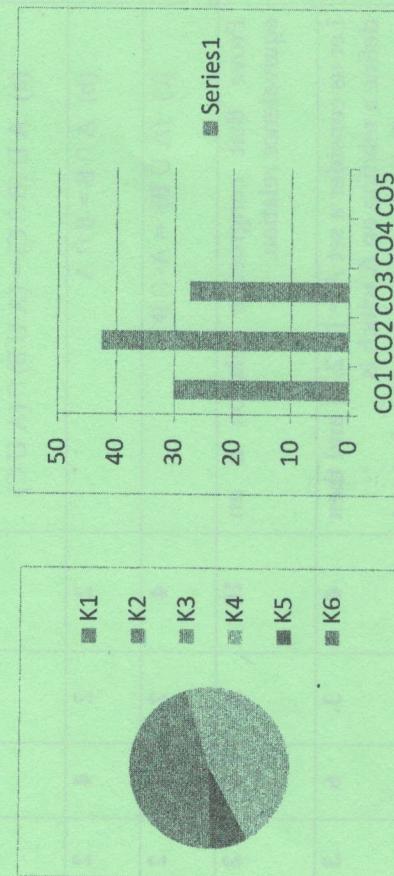


CO- Course Outcomes, KL- Knowledge Level, PO – Program Outcome

Course Outcomes	CO1	30	Knowledge Level	K1	4
	CO2	42.5		K2	16
	CO3	27.5		K3	0
	CO4	0		K4	47
	CO5	0		K5	7.5
				K6	25.5



Branch	Computer Science & Engineering	Program	B.TECH
Course Name	Discrete Mathematics	Semester	IV
Course Code	BTE24065	Year	2022/Even

- Time: 3 Hour Maximum Marks : 70
- Start writing from 2nd page onwards; don't Write On The 1st Page Backside
  - Answer all Questions of Section A (Compulsory)
  - Answer Any Four out of Six of Section B
  - Answer Any Three out of Five of Section C
  - Possession of Mobile Phones or any kind of Written Material, Arguments with the Invigilator or Discussing with Co-Student will comes under Unfair Means and will Result in the Cancellation of the Papers.

Knowledge Level (KL)

K1 : Remembering  
K2 : Understanding  
K3 : Applying  
K4 : Analysing  
K5 : Evaluating  
K6 : Creating

### Section A (Each question Carry 02 Marks from Q1a to Q1j) – 20 Marks

Q. No.1	Questions	Marks	COs	KL	PO
1a.	Define intersection of two sets.	2		1	1
1b.	Define subset of a set.	2		1	1
1c.	Explain symmetric property of relation.	2		2	1
1d.	Explain injective function.	2		1	1
1e.	Explain onto mapping.	2		2	1
1f.	What is meant by a denumerable set?	2		1	2
1g.	When a set is said to be uncountable?	2		1	2
1h.	Explain closure property.	2		1	2

<b>1i.</b>	Explain residue class addition.	2	1	2	1	1
<b>1j.</b>	Explain cyclic group.	2	1	2	1	1

**Section B (Answer any FOUR out of SIX) – 20 Marks (Each question Carry 5 Marks)**

Q NO	Questions	Marks	COS	KL	PO
2a.	If $A = \{2, 3, 5\}$ and $B = \{1, 2, 3, 4\}$ , then find (a) $(A - B) \cup (B - A)$	3	2	5	2
2b.	(a) $B \times A$	2	2	5	2
3a.	Define an equivalence relation and mention one such relation.	5	1	6	1
4a.	Explain with example the composition of two mappings.	5	1	6	1
5a.	Let $A = \{2, 3, 5\}$ and $B = \{1, 3, 5, 7\}$ are two given sets. If $f_1$ and $f_2$ be two correspondences defined from set A to set B given as $f_1 = \{(2, 1), (3, 3), (3, 5), (5, 5)\}$ and $f_2 = \{(2, 1), (3, 1), (5, 5)\}$ . Now answer the following: a) Is $f_1$ a function from A to B? Give reason. b) Represent $f_2$ diagrammatically.	2.5	2	5	2
6a.	(a) Complete the following composition table (where + denotes ordinary addition):	3	3	6	3
6b.	(b) Does your completed composition table indicate that the operation + is commutative?	2	3	4	3

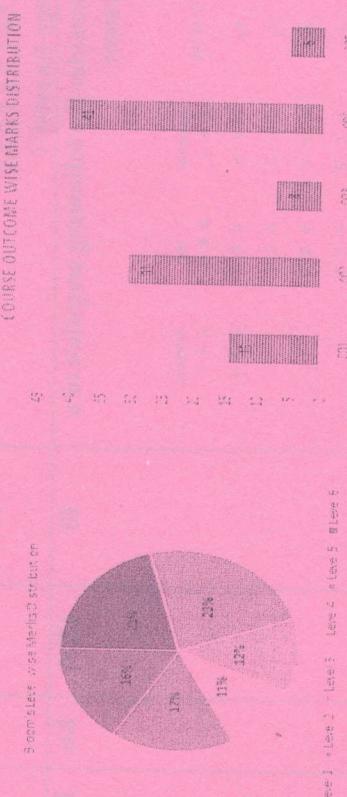
7. Prove that in a group the inverse of an element is unique.

**Section C (Answer any THREE out of FIVE) – 30 Marks-(Each question Carry 10 Marks)**

Q NO	Questions	Marks	COS	KL	PO
8a.	Prove the following for any three sets A, B and C: (a) $A \cup (B \cap C) = (A \cup B) \cap (A \cup C)$	4	2	4	2
8b.	(b) $A \cap B = B \cap A$	2	2	4	2
8c.	(c) $(A \cup B)^c = A^c \cap B^c$	4	2	4	2
9.	Prove that congruence relation is an equivalence relation.	10	2	4	2
10a.	Let us consider a set $A = \{1, 2, 3\}$ and then define a relation on A which is (a) Reflexive and symmetric but not transitive.	4	3	6	3
10b.	(b) Reflexive but neither symmetric nor transitive.	3	3	6	3
10c.	(c) Symmetric but neither reflexive nor transitive.	3	3	6	3
11.	Prove that the set of all rational numbers is denumerable.	10	2	4	2
12.	Check if the set of residue class multiplication modulo 6 forms an abelian group?	10	3	4	3

		<b>ARKA JAIN</b> <b>University</b> Jharkhand		END TERM EXAMINATION	
		B.Tech		Program	
		Branch	Computer Science & Engineering	Semester	IV
		Course Name	Operating System	Year	2022/Even
		Course Code	BTE24067		
12a.		Define seek time and latency time. List two ways of allocating storage and give advantages of each.		4	CO5 K4 PO2
12b.		Describe any two: i. race condition ii. Shared memory model iii. Monolithic Kernel		6	CO2 K1 PO1
CO- Course Outcomes, KL- Knowledge Level, PO – Program Outcome					
Course Outcomes	CO1	To Identify mechanisms to create processes and threads.			
	CO2	Develop algorithms for process scheduling for a given specification of CPU utilization, Throughput, Turnaround Time, Waiting Time, Response Time			
	CO3	For a given specification of memory organization develop the techniques for optimally allocating memory to processes by increasing memory utilization and for improving the access time			
	CO4	Design and implement file management system			
	CO5	Develop the I/O management functions in OS as part of a uniform device abstraction by performing operations for synchronization between CPU and I/O controllers.			
Time: 3 Hour Maximum Marks : 70		<ul style="list-style-type: none"> <li>• Start writing from 2nd page onwards; <u>don't Write On The 1st Page Backside</u></li> <li>• Answer all Questions of Section A (Compulsory)</li> <li>• Answer Any Four out of Six of Section B</li> <li>• Answer Any Three out of Five of Section C</li> <li>• Possession of Mobile Phones or any kind of <u>Written Material</u> Arguments with the Invigilator or Discussing with Co-Student will comes under <u>Unfair Means</u> and will <u>Result</u> in the Cancellation of the Papers.</li> </ul>			
Knowledge Level (KL)		K1 : Remembering	K3 : Applying	K5 : Evaluating	
Section A (Each question Carry 02 Marks from Q1a to Q1j) – 20 Marks		K2 : Understanding	K4 : Analysing	K6 : Creating	
Q. No.1					
QUESTIONS					
Marks					
CO1 CO2 CO3 CO4 CO5 K1 K2 PO1					
1a. What is Belady's anomaly?					
1b. Compare and contrast DMA and Cache memory.					
1c. Defend the statement timesharing differs from multiprogramming. If so, how?					
1d. What are the objectives of Operating System?					
1e. Explain the terms deadlock and livelock.					
1f. Name the 4 necessary conditions for deadlock situation to arise.					
1g. Differentiate between internal and external fragmentation.					
1h. Identify what virtual machine is and what are its advantages.					
1i. What is a kernel? Name any two types of kernel.					

Course Outcomes	CO1	CO2	CO3	CO4	CO5	KL	PO
12a.	Define seek time and latency time. List two ways of allocating storage and give advantages of each.					4	CO5 K4 PO2
12b.	Describe any two: i. race condition ii. Shared memory model iii. Monolithic Kernel					6	CO2 K1 PO1
CO- Course Outcomes, KL- Knowledge Level, PO – Program Outcome	CO1	CO2	CO3	CO4	CO5	KL	PO



- 1j.** Elaborate the terms: IPC, RPC, FCFS, LRU

Section B (Answer any FOUR out of SIX) - 20 Marks (Each question 5 Marks)					
Q. No.	QUESTIONS	Marks	COs	KL	PO
2a.	Compare the working of C-SCAN and SCAN disk scheduling.	3	CO4	K2	PO4
2b.	Throw some light on Critical Section problem.	2	CO1	K4	PO4
3a.	Differentiate between Deadlock and Starvation. How can we resolve starvation?	3	CO4	K3	PO3
3b.	Discuss two solutions to solve the critical section problem.	2	CO1	K4	PO3
4.	For the given set of processes, calculate the average Turn Around Time and Average Waiting Time using Priority scheduling.	5	CO2	K5	PO4

Waiting Time using Priority

P_id	AT	BT	Priority
P1	1	4	1
P2	2	5	2
P3	3	2	3
P4	4	1	4
P5	5	6	5
P6	6	3	6

- 5a. What is PCB?  
5b. Mention the jobs performed by a kernel. Also provide 2 differences between monolithic and micro kernels.

- 6a. For the given set of processes, calculate the average Turn Around Time and Average Waiting Time using FCFS scheduling.

P_id	AT	BT
P1	3	1
P2	1	4
P3	4	2
P4	0	6
P5	2	3

- 6b. In relation to operating system, define thread.  
7a. What is disk scheduling?  
7b. Compare FCFS and SCAN disk scheduling algorithms.

1. Calculate the content of need matrix.

2. Is the system in a Safe State? If yes, mention the sequence.

Section C (Answer any THREE out of FIVE) - 30 Marks-(Each question Carry 10 Marks)

Q. No.	QUESTIONS	Marks	COs	KL	PO
8a.	With reference to classical IPC problems, discuss Readers Writers problem. Also mention the feasible solution for the same.	5	CO3	K3	PO3
8b.	What is booting? Explain the life cycle of a thread.	5	CO1	K2	PO1
9a.	What is demand paging? Outline about virtual memory and its advantages.	4	CO4	K4	PO2
9b.	Using Optimal page replacement scheme, calculate the page fault, miss ratio, and hit ratio for the given reference string: 4,7,6,1,7,6,1,2,7,2. Page frames=4	6	CO4	K5	PO4
10a.	What is Convoy effect? Show an example to justify your answer.	4	CO2	K2	PO3
10b.	What is paging? Using FIFO page replacement scheme, calculate the page fault, miss ratio, and hit ratio for the given reference string: 4,7,6,1,7,6,1,2,7,2. Page frames=3	6	CO4	K5	PO4
11.	Consider the following snapshot of a system:	10	CO4	K6	PO9

Processes	Allocation			Available
	A	B	C	
P0	1	1	2	4 3 3
P1	2	1	2	3 2 2
P2	4	0	1	9 0 2
P3	0	2	0	7 5 3
P4	1	1	2	1 1 2

1. Calculate the content of need matrix.  
2. Is the system in a Safe State? If yes, mention the sequence.

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CO- Course Outcomes, KL- Knowledge Level, PO – Program Outcome

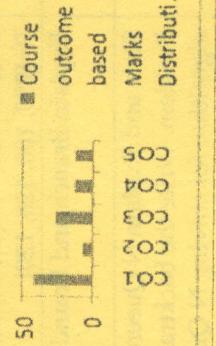
Course Outcomes	CO1	Formulate simple algorithms for arithmetic and logical problems.
	CO2	Describe the divide-and-conquer paradigm and explain when an algorithmic design situation calls for it. Synthesize divide-and-conquer algorithms.
	CO3	Describe the greedy paradigm and explain when an algorithmic design situation calls for it. For a given problem develop the greedy algorithms
	CO4	For a given model engineering problem model it using graph and write the corresponding algorithm to solve the problems.
	CO5	To decompose a problem into functions and synthesize a complete program using divide and conquer approach

Branch	Computer Science & Engineering	Program	B.Tech						
Course Name	Design and Analysis of Algorithms	Semester	IV						
Course Code	BTE24068	Year	2022/Even						
Time: 3 Hour Maximum Marks : 70	<ul style="list-style-type: none"> <li>Start writing from 2nd page onwards; <u>don't Write On The 1st Page Backside</u></li> <li>Answer all Questions of Section A (Compulsory)</li> <li>Answer Any Four out of Six of Section B</li> <li>Answer Any Three out of Five of Section C</li> <li>Possession of <u>Mobile Phones</u> or any kind of <u>Written Material</u>, <u>Arguments with the Invigilator or Discussing with Co-Student</u> will comes under <u>Unfair Means</u> and will <u>Result</u> in the <u>Cancellation</u> of the <u>Papers</u>.</li> </ul>								
Knowledge Level (KL)	<table border="1"> <tr> <td>K1 : Remembering</td> <td>K3 : Applying</td> <td>K5 : Evaluating</td> </tr> <tr> <td>K2 : Understanding</td> <td>K4 : Analysing</td> <td>K6 : Creating</td> </tr> </table>	K1 : Remembering	K3 : Applying	K5 : Evaluating	K2 : Understanding	K4 : Analysing	K6 : Creating		
K1 : Remembering	K3 : Applying	K5 : Evaluating							
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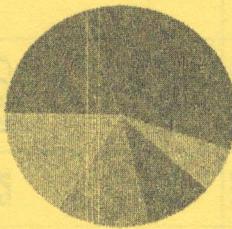
### **Section A (Each question Carry 02 Marks from Q1a to Q1j) - 20 Marks**

Q. No.1	QUESTIONS	Marks	COs	KL	PO
1a.	Discuss the characteristics of a good Algorithm.	2 [1]	CO	K1	PO [2]
1b.	Differentiate Greedy Programming vs Dynamic Programming.	2 [3]	CO	K4	PO [3]
1c.	Define Spanning Tree.	2 [4]	CO	K1	PO [1]
1d.	What is Recursion?	2 [1]	CO	K2	PO [2]
1e.	Define Depth First search in a graph.	2 [4]	CO	K1	PO [1]

### **Course outcome based Marks Distribution**



### **Bloom's Level Marks Distribution**



**Section C (Answer any THREE out of FIVE) - 30 Marks-(Each question Carry 10 Marks)**

Q. No.	QUESTIONS	Marks	COs	KL	PO	Q. No	QUESTIONS	Marks	COs	KL	PO
1f.	Explain the term Chromatic Number of a graph with example.	2	CO [4]	K6	PO [1]	8a.	Explain Greedy programming approach.	2	CO[2]	K1	PO [2]
1g.	Evaluate and write the recurrence relation capturing the optimal time of the Tower of Hanoi problem with n discs.	2	CO [1]	K5	PO [2]	8b.	Find single source (1) shortest path for the given graph using Dijkstra's Algorithm.	8	CO[2]	K5	PO [2]
1h.	Determine the worst case time complexity of selection sort?	2	CO [1]	K5	PO [2]						
1i.	Find the O-notation for the following function. $f(n)=4n^3+2n+3$	2	CO [1]	K5	PO [2]						
1j.	Define Big O notation.	2	CO [1]	K1	PO [2]						
						9a.	Explain Matrix Chain Multiplication problem.	3	CO[1]	K2	PO [2]
						9b.	Write Dynamic programming for matrix chain multiplication problem.	4	CO[3]	K2	PO [3]
						9c.	Write Stassen's matrix multiplication algorithm.	3	CO[3]	K3	PO [3]
						10a.	Find the optimal solution for the following fractional Knapsack problem. n=4, m = 60, W={40, 10, 20, 24} and P={280, 100, 120, 120}	8	CO[3]	K5	PO [3]
						10b.	Explain Branch and Bound method.	2	CO[3]	K1	PO [3]
						11a.	State and Explain N Queens Problem. Write the backtracking algorithm for solving N Queens problem.	8	CO[3]	K6	PO [3]
						11b.	Show the state space tree for 4 Queens problem.	2	CO[3]	K6	PO [3]
						12a.	Define NP- Hard and NP - Complete Problems.	5	CO[5]	K4	PO [4]
						12b.	What are the steps used to show a given problem is NP-Complete?	5	CO[1]	K2	PO [4]

**Section B (Answer any FOUR out of SIX) - 20 Marks (Each question 5 Marks)**

Q. No	QUESTION	Marks	COs	KL	PO
2a.	Differentiate Recursion and Iteration.	2	CO[1]	K4	PO [2]
2b.	Write a Recursive Function to determine the factorial of a number.	3	CO[1]	K3	PO [2]
3.	Solve the following Recurrence equation by substitution method. $T(n)=1,$ $\quad \quad \quad \text{if } n=1$ $\quad \quad \quad =n*T(n-1)$ $\quad \quad \quad \text{if } n>1$	5	CO[1]	K6	PO [2]
4.	Define Tower-of-Hanoi Problem and write the algorithm.	5	CO[1]	K2	PO [2]
5.	Define Path, cycle and Planar graph with appropriate diagram.	5	CO[4]	K2	PO [1]
6.	Illustrate 0/1 knapsack problem with suitable example. Which algorithm strategy is used to solve this problem?	5	CO[5]	K2	PO [4]
7.	Write the algorithm of insertion sort and determine its time complexity.	5	CO[1]	K2	PO [2]

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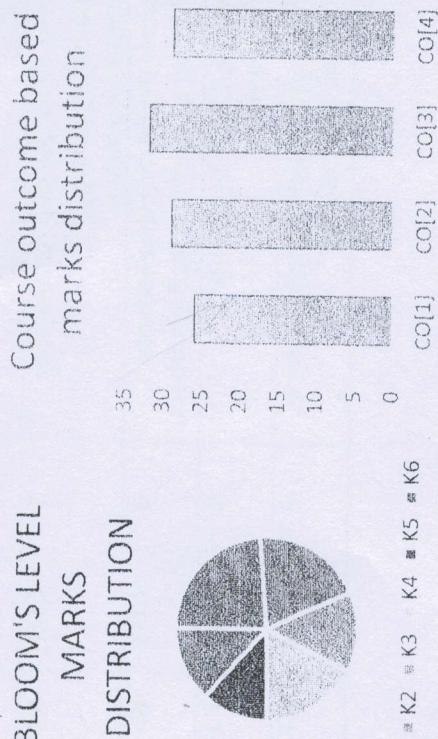
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END TERM  
EXAMINATION

			CO	K4	PO3
12a.	What is DMA? Describe how DMA is used to transfer data from peripherals.	4	CO2	K4	PO3
12b.	What do you mean by Input-Output (I/O) processor?	2	CO2	K2	PO3
12c.	Formulate the performance of CPU.	4	CO4	K6	PO1
CO- Course Outcomes, KL- Knowledge Level, PO - Program Outcome					
Course Outcomes	CO1	Draw the functional block diagram of a single bus architecture of a computer and describe the function of the instruction execution cycle			
	CO2	Write assembly language program for specified microprocessor for computing 16-bit multiplication, division and I/O device interface (ADC, Control circuit, serial port communication).			
	CO3	Write a flowchart for Concurrent access to memory and cache coherence in Parallel Processors and describe the process			
	CO4	Given a CPU organization and instruction, design a memory module and analyze its operation by interfacing with the CPU			

Branch	Computer Science & Engineering	Program	B.TECH
Course Name	Computer Organisation and Architecture	Semester	IV
Course Code	BTE24066	Year	2022/Even
Time: 3 Hour Maximum Marks : 70	<ul style="list-style-type: none"> <li>Start writing from 2nd page onwards; <u>don't Write On The 1st Page Backside</u></li> <li>Answer all Questions of Section A (Compulsory)</li> <li>Answer Any Four out of Six of Section B</li> <li>Answer Any Three out of Five of Section C</li> <li>Possession of Mobile Phones or any kind of Written Material Arguments with the Invigilator or Discussing with Co-Student will comes under <u>Unfair Means</u> and will <u>Result</u> in the Cancellation of the Papers.</li> </ul>		
Knowledge Level (KL)	<p>K1 : Remembering</p> <p>K2 : Understanding</p>	<p>K3 : Applying</p> <p>K4 : Analysing</p>	<p>K5 : Evaluating</p> <p>K6 : Creating</p>
Section A (Each question Carry 02 Marks from Q1a to Q1j) – 20 Marks			

Q. No.1	Questions	Marks	COs	KL	PO
1a.	List the functions of I/O Interface.	2	CO 2	K2	PO 3
1b.	Describe the functions of instructions.	2	CO 1	K1	PO 1
1c.	Differentiate between RISC and CISC.	2	CO 2	K2	PO 3
1d.	What is effective address?	2	CO 1	K1	PO 7
1e.	Differentiate SRAM and DRAM	2	CO 4	K2	PO 1
1f.	Explain the cache memory.	2	CO 3	K2	PO 2
1g.	Illustrate the uses of adder. Give its types.	2	CO 2	K2	PO 3
1h.	What you understand by multiprogramming?	2	CO 2	K2	PO 3
1i.	Evaluate the concurrent access of cache memory.	2	CO 3	K5	PO 2



<b>1j.</b>	Give an analysis report on DMA.	2	CO 2	K 4	PO 3
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**Section B (Answer any Four out of six) – 20 Marks (Each question Carry 5 Marks)**

QNO.	Questions	Marks	COs	KL	PO
<b>2a.</b>	Draw a block diagram of a Computer's CPU showing all the components.	3	CO4	K4	PO1
<b>2b.</b>	Explain the functional units of digital system and their interconnections.	2	CO2	K2	PO3
<b>3a.</b>	What is a bus in a digital computer? Write all the types.	3	CO2	K1	PO3
<b>3b.</b>	What are the different categories of memory?	2	CO3	K1	PO7
<b>4a.</b>	If an instruction contains four addresses, what might be the purpose of each address?	3	CO1	K3	PO7
<b>4b.</b>	How do ALU perform the multiplication of digital numbers?	2	CO4	K1	PO1
<b>5a.</b>	Write the booth algorithm with its flowchart.	3	CO2	K5	PO3
<b>5b.</b>	Explain pipeline concept.	2	CO3	K1	PO2
<b>6a.</b>	Analyse the hazards of pipelining.	3	CO3	K4	PO2
<b>6b.</b>	Write in detail the replacement policies of memory.	2	CO4	K2	PO1
<b>7a.</b>	Write the different levels of cache memory.	3	CO3	K1	PO2
<b>7b.</b>	Compose the factors that affect performance of a CPU.	2	CO4	K1	PO1
<b>Section C (Answer any three out of Five) – 30 Marks-(Each question Carry 10 Marks)</b>					
QNO.	Questions	Marks	COs	KL	PO
<b>8a.</b>	Write the algorithm for restoring way of division.	3	CO1	K2	PO7
<b>8b.</b>	Apply and multiply (Use booth algorithm). i) $4 \times 5$ ii) $-6 \times 3$	4	CO1	K	PO7
<b>11c.</b>	What is parallelism and pipelining in computer architecture?	2	CO4	K1	PO1

<b>8c.</b>	What are the advantages and disadvantages of using a variable-length instruction format?	3	CO1	K1	PO7
<b>9a.</b>	Explain how arithmetic addition and multiplication is performed in floating point numbers.	3	CO1	K2	PO7
<b>9b.</b>	What is parallel processing? Explain the creation of instruction pipelining.	3	CO3	K6	PO2
<b>9c.</b>	Draw a block diagram of a computer's CPU showing all the basic building blocks such as program counter, accumulator, address and data registers, instruction register, control unit etc., and describe how such an arrangement can work as a computer, if connected properly to memory, input/output etc.	4	CO4	K4	PO1
<b>10a.</b>	Explain the following addressing modes with the help of an example each: i. Direct ii. Register indirect iii. Implied iv. Immediate	4	CO2	K1	PO3
<b>10b.</b>	Show the multiplication process using Booth's algorithm when the following numbers are multiplied: $(-13) \times (+8)$	3	CO1	K5	PO7
<b>10c.</b>	Write down the step for restoring and non-restoring of division operations.	3	CO2	K2	PO3
<b>11a.</b>	Assess the relationship between physical address and logical address.	4	CO3	K6	PO2
<b>11b.</b>	What is CISC? Explain its characteristics.	4	CO4	K2	PO1
<b>11c.</b>	What is parallelism and pipelining in computer architecture?	2	CO4	K1	PO1

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**END TERM  
EXAMINATION**

Branch	Computer Science Engineering	Program	B.TECH
Course Name	Microprocessor and Microcontroller	Semester	IV
Course Code	BTE24393	Year	2022/Even
Time: 3 Hour Maximum Marks : 70	<ul style="list-style-type: none"> <li>• Start writing from 2nd page onwards; <u>don't Write On The 1st Page Backside</u></li> <li>• Answer all Questions of Section A (Compulsory)</li> <li>• Answer Any Four out of Six of Section B</li> <li>• Answer Any Three out of Five of Section C</li> <li>• Possession of Mobile Phones or any kind of <u>Written Material</u>, <u>Arguments with the Invigilator or Discussing with Co-Student</u> will comes under <u>Unfair Means</u> and will <u>Result</u> in the <u>Cancellation of the Papers</u>.</li> </ul>		
Knowledge Level (KL)	K1 : Remembering  K2 : Understanding	K3 : Applying  K4 : Analysing	K5 : Evaluating  K6 : Creating

**Section A (Each question Carry 02 Marks from Q1a to Q1j) – 20 Marks**

Q. No.1	Questions	Marks	COs	KL	PO
1a.	Discuss the utility of program counter register in 8085 microprocessor	2	CO1	K4	PO2
1b.	Identify the addressing mode of instruction LXI RP, 16 bit . also explain the instruction.	2	CO2	K3	PO1
1c.	Explain the following instructions with suitable example of each (i) MVI (ii) MOV	2	CO3	K2	PO3
1d.	What are the different types of flags in 8085 microprocessor?	2	CO3	K1	PO4
1e.	What is Tri-state logic?	2	CO4	K1	PO4
1f.	Explain the function of ALE and IO/ $\overline{M}$ signals of the 8085 microprocessor.	2	CO4	K2	PO5
1g.	Write assembly level program to add two 8 bit numbers.	2	CO4	K3	PO4

<b>1h.</b>	What happens when HALT instruction is executed in processor?	2	CO1	K4	PO2
<b>1i.</b>	Explain the instruction LDAX Rp	2	CO1	K2	PO3
<b>1j.</b>	Explain arithmetic instructions ADD M	2	CO1	K2	PO2

**Section B (Answer any FOUR out of SIX) – 20 Marks (Each question Carry 5 Marks)**

Q NO	Questions	Marks	COs	KL	PO
2	A microprocessor has frequency of 5 MHz and an instruction required 7 T state to execute. Find the time taken by the processor to execute that instruction	5	CO4	K4	PO2
3	Draw the pin configuration of 8255 controller. Explain each pin briefly.	5	CO4	K3	PO1
4	Construct a neat and clean diagram for 8085 microprocessor Pin out and signals.	5	CO3	K3	PO3
5	Draw functional block diagram of 8085 microprocessor.	5	CO5	K5	PO3
6	Describe the register organization in 8085 microprocessor.	5	CO1	K4	PO1
7	Describe each type of interrupts of 8085 microprocessor with suitable example?	5	CO2	K3	PO2

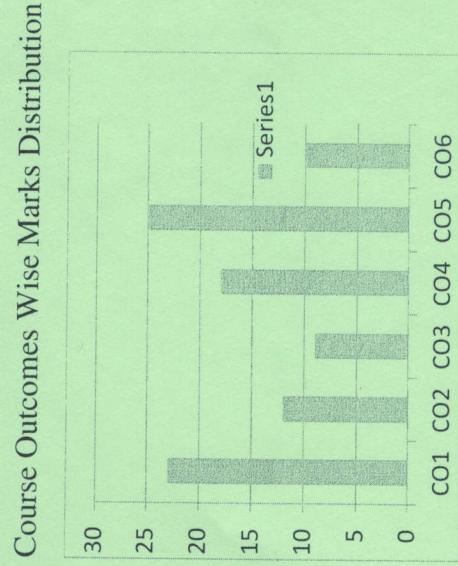
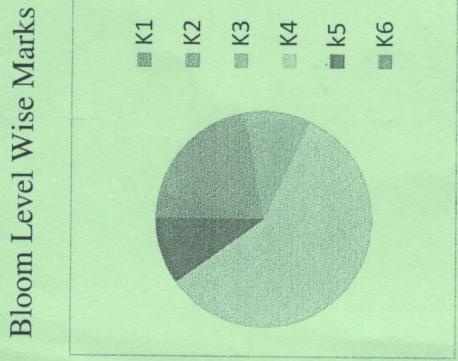
**Section C (Answer any THREE out of FIVE) – 30 Marks-(Each question Carry 10 Marks)**

Q NO	Questions	Marks	COs	KL	PO
8.	What are Mnemonics? Write algorithm and assembly level program to find largest number in an array	10	CO5	K4	PO2
9	What are main features of 8051 microcontroller? Draw functional block diagram of 8051 microcontroller.	10	CO1	K2	PO4
10	Discuss pin configuration of 8251 USART chip also discuss functional block diagram.	10	CO2	K4	PO2
11	Draw and discuss the architecture and pin configuration of 8257 DMA controller	10	CO5	K4	PO3
12	Draw the timing diagram for execution of the instruction STA 8000H.	10	CO6	K4	PO2

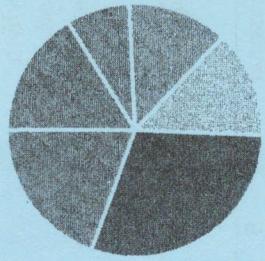
CO- Course Outcomes, KL- Knowledge Level, PO - Program Outcome

		CO1	Assess and solve basic binary math operations using the microprocessor and explain the microprocessor's and Microcontroller's internal architecture and its operation within the area of manufacturing and performance		
		CO2	Apply knowledge and demonstrate programming proficiency using the various addressing modes and data transfer instructions of the target microprocessor and microcontroller.		

		CO3	Compare accepted standards and guidelines to select appropriate Microprocessor (8085 & 8086) and Microcontroller to meet specified performance requirements		
		CO4	Analyze assembly language programs; select appropriate assemble into machine a cross assembler utility of a microprocessor and microcontroller.		
		CO5	Design electrical circuitry to the Microprocessor I/O ports in order to interface the processor to external devices.		



Bloom's Level wise Marks  
Distribution



K1 ■ K2 ■ K3 ■ K4 ■ K5 ■ K6

Course Outcome wise  
Marks Distribution

25

20

15

10

5

0

ARKAJAIN University Jharkhand		END TERM EXAMINATION	
Branch	Computer Science & Engineering	Program	B.TECH
Course Name	Software Engineering	Semester	IV
Course Code	BTE24394	Year	2022/Even
Time: 3 Hour Maximum Marks : 70			<ul style="list-style-type: none"> <li>• Start writing from 2nd page onwards; <u>don't Write On The 1st Page Backside</u></li> <li>• Answer all Questions of Section A (Compulsory)</li> <li>• Answer Any Four out of Six of Section B</li> <li>• Answer Any Three out of Five of Section C</li> <li>• Possession of Mobile Phones or any kind of Written Material, Arguments with the Invigilator or Discussing with Co-Student will comes under <u>Unfair Means</u> and will <u>Result</u> in the <u>Cancellation</u> of the Papers.</li> </ul>
Knowledge Level (KL)	K1 : Remembering K2 : Understanding K3 : Applying K4 : Analysing K5 : Evaluating K6 : Creating		

Section A (Each question Carry 02 Marks from Q1a to Q1j) – 20 Marks

Q. No.1	Questions	Marks	COs	KL	PO
1a.	Demonstrate your understanding of umbrella activities of a Software process.	2	CO1	K3	PO3
1b.	Summarize the pros and cons of iterative software development model.	2	CO1	K5	PO3
1c.	Give a use case diagram for an online shopping which should provide provisions for registering authenticating the customers and also online payment through any payment gateway like PayPal	2	CO1	K2	PO2
1d.	How requirements are classified? List them with an example for each.	2	CO1	K3	PO1
1e.	A system must be loosely coupled and highly cohesive'. Justify	2	CO2	K5	PO1
1f.	Classify the user interface design steps.	2	CO2	K3	PO3

<b>1g.</b>	Summarize various testing strategies for conventional software?	2	CO4	K2	PO2
<b>1h.</b>	Analyse on what is a "good" test and List two principles of good design.	2	CO4	K4	PO2
<b>1i.</b>	List out the principles of project scheduling.	2	CO5	K1	PO11
<b>1j.</b>	Generalize on the concept of project metrics.	2	CO3	K6	PO11

**Section B (Answer any FOUR out of SIX) – 20 Marks (Each question Carry 5 Marks)**

Q NO	Questions	Marks	COs	KL	PO
2.	Explain at least one scenario where RAD model would be applicable and not the waterfall model.	5	CO1	K4	PO3
3a.	Compose your view about agile software development.	3	CO1	K6	PO3
3b.	How will you classify the requirement types of a project, give example?	2	CO2	K6	PO4
4a.	What is feasibility study? How it helps in requirement engineering process.	3	CO2	K6	PO4
4b.	Discuss the component-level design guidelines.	2	CO2	K1	PO3
5.	What is the purpose of data flow diagrams? What are the notations used for the same?	5	CO5	K4	PO5
6a.	Summarize on Top-down Integration testing and Bottom -up integration testing.	3	CO4	K2	PO1
6b.	What conclusions can you draw from regression testing? Support your answer with a neat sketch.	2	CO4	K5	PO1
7a.	Demonstrate Function Point estimation.	3	CO3	K3	PO1
7b.	Outline the importance of "project scheduling and use of Gantt charts"	2	CO5	K3	PO1

<b>Section C (Answer any THREE out of FIVE) – 30 Marks-(Each question Carry 10 Marks)</b>	<b>CO- Course Outcomes, KL- Knowledge Level, PO – Program Outcome</b>
7a.	CO1 Interpret, plan, and develop the frame work of a software engineering project
7b.	CO2 Monitor & manage the risk during the design of software project.
	CO3 Calculate the cost of software, using cost estimation models such as COCOMO II.
	CO4 Identify and apply testing strategies & methods on software projects.
	CO5 Implement clean room techniques to develop as well as maintain software throughout its lifetime.

<b>1g.</b>	organization. A Client approached you for a software solution the problems stated by the client have uncertainties which lead to loss if it not planned and solved which software development model you will suggest for this project -justify. Explain that model With its pros and cons and neat sketch.	5	CO2	K5	PO1
<b>9a.</b>	Write short notes on aspect oriented software development.	5	CO1	K5	PO3
<b>9b.</b>	Explain in detail about personal process models and team process models.	5	CO5	K5	PO5
<b>10a.</b>	Model a Dataflow diagram for a "Library Management System".	5	CO5	K5	PO4
<b>10b.</b>	State and explain the functional requirements you are considering for a "Library Management System".	5	CO4	K6	PO3
<b>11a.</b>	Generalize on the concept of user interface design pattern.	5	CO2	K6	PO3
<b>11b.</b>	Develop the design issues in interface design.	5	CO4	K6	PO3
<b>12a.</b>	Describe in detail about Process Metrics.	5	CO3	K1	PO11
<b>12b.</b>	How should we use metrics during the project itself?	5	CO3	K1	PO11